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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/981,291	10/16/2001	David William Goodwin	083818 0269265	4990

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EXAMINER	
ZHEN, WEI Y	

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/981,291	GOODWIN ET AL.	
	Examiner	Art Unit	
	Wei Y Zhen	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4,6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the preliminary amendment filed on 4/14/2004.

2. Claims 1-12, 14-33 are pending.

3. Claim 13 has been canceled.

Information Disclosure Statement

4. The information disclosure statements (IDS) submitted on 5/15/2002 (paper no. 4) and 4/6/2004 (paper no. 6) are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-2, 14-29 are rejected under 35 U.S.C. 102(a) as being anticipated by "ASIP Design Methodologies: Survey and Issues" by Jain et al (Art of Record).

As per claim 1, Jain et al discloses

means for receiving at least one software program written in a high level language (p. 76 right column, "application analysis" and p. 77, Fig. 1)

means for automatically generating an instruction set architecture optimized for executing that program, wherein the instruction set architecture is represented as a set of configurations

containing one or more extension instructions based on instructions in an existing standard or existing user defined instruction set architecture (p. 77, left column, "Architecture Design Space Exploration" and "Instruction Set Generation" and Fig. 1).

As per claim 2, Jain et al discloses the extension instructions operates on states and register files in the existing standard of existing user-defined instructions set architectures (p. 77, left column, "Architecture Design Space Exploration" and "Instruction Set Generation" and Fig. 1).

As per claim 14, Jain et al discloses instruction set architecture generation is guided by analysis information gathered from the at least one software program; and the analysis information is gathered for each region of code that could get a performance improvement from a generated instruction set algorithm (p. 76, right column, "application analysis").

As per claim 15, Jain et al discloses information includes an execution count of each region as determined from real or estimated profiling information (p. 77, right column, "Application Analysis" and p. 78, right column, "Performance Estimation").

As per claim 16, Jain et al discloses the analysis information includes an execution count of each region as determined from user-supplied directives information (p. 77, right column, "Application Analysis" and p. 78, right column, "Performance Estimation").

As per claim 17, Jain et al discloses the analysis information includes a dependence graph of each region (p. 77, right column, "Application Analysis" and p. 78, right column, "Performance Estimation").

As per claim 18, Jain et al discloses the analysis information includes a set of operation vector lengths that can be used to improve performance of each region (p. 77, right column, "Application Analysis" and p. 78, right column, "Performance Estimation").

As per claim 19, Jain et al discloses each region is evaluated with a set of instruction set architecture configurations to determine a performance improvement that would result if instructions, operations, register files, and states represented by the configuration could be used for the region (p. 77, right column, "Application Analysis" and p. 78, right column, "Performance Estimation").

As per claim 20, Jain et al discloses instruction set architecture generation uses as a guideline an estimate of hardware cost of each instruction set architecture configuration that includes a cost of logic necessary to implement instructions, operations, register files, and state represented by the configuration; and the hardware cost and performance improvement of each instruction set architecture configuration for each region is used to determine a set of instruction set architecture configurations that together describe the generated instruction set architecture such that the performance improvement of the software program(s) is increased as much as possible while the hardware cost of the generated instruction set architecture does not exceed a

cost budget (p. 78, right column to p. 79, left column, "Performance Estimation").

As per claim 21, Jain et al discloses instruction set architecture generation uses as a guideline an estimate of hardware cost of each instruction set architecture configuration that includes a cost of logic necessary to implement instructions, operations, register files, and state represented by the configuration; and the hardware cost and performance improvement of each instruction set architecture configuration for each region is used to determine the set of instruction set architecture configurations that together describe the generated instruction set architecture such that the hardware cost of the generated instruction set architecture is as small as possible while providing a performance improvement that is greater or equal to a performance goal (p. 78, right column to p. 79, left column, "Performance Estimation").

As per claim 22, Jain et al discloses the hardware cost and performance improvement of each instruction set architecture hardware configuration for each region is used to determine the set of instruction set architecture configurations that together describe the generated instruction set architecture such that the hardware cost of the generated instruction set architecture is smaller than a predetermined function of the performance improvement (p. 78, right column to p. 79, left column, "Performance Estimation").

As per claim 23, Jain et al disclose a performance improvement provided by a particular instruction set architecture configuration for a particular region is determined by an instruction scheduling algorithm operating on a modified dependence graph of the region (p. 77, right column and p. 78, right column to p. 79, left column, "Performance Estimation").

As per claim 24, Jain et al discloses the dependence graph is modified to replicate operations with an operation width that is less than one (p. 77, right column and p. 78, right column to p. 79, left column, "Performance Estimation").

As per claim 25, Jain et al discloses the dependence graph is modified to replace groups of operations with a single fused operation (p. 77, right column and p. 78, right column to p. 79, left column, "Performance Estimation").

As per claim 26, Jain et al discloses the performance improvement provided by a particular instruction set architecture configuration for a particular region is determined using resource limits (p. 77, right column and p. 78, right column to p. 79, left column, "Performance Estimation").

As per claim 27, Jain et al discloses instruction set architecture generation is guided by an estimate of hardware cost of each instruction set architecture configuration that includes a cost of logic necessary to implement instructions, operations, register files, and state represented by the configuration (p. 77, right column and p. 78, right column to p. 79, left column, "Performance Estimation").

As per claim 28, Jain et al discloses wherein the hardware cost is estimated by adding hardware costs of components present in the instruction set architecture configuration (p. 77, right column and p. 78, right column to p. 79, left column, "Performance Estimation").

As per claim 29, Jain et al discloses the hardware cost is reduced to represent reduced logic necessary when specialized operations replace generic operations (p. 77, right column and p. 78, right column to p. 79, left column, "Performance Estimation").

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-12, 30-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over "ASIP Design Methodologies: Survey and Issues" by Jain et al (Art of Record).

As per claims 3-12, Jain et al does not explicitly discloses the extension instructions contain vectorized versions of the existing instructions, or VLIW combinations of the existing instructions, or fused combinations of the existing instructions, or specialized versions of the existing instructions, or vectorized versions of operations supported by the high level language or VLIW combinations of operations supported by the high level language, or fused combinations of operations supported by the high level language or specialized versions of operations supported by the high level language, or at least two of vectorized, VLIW, fused and specialized versions of the existing instructions, or at least two of vectorized, VLIW, fused and specialized versions of operations supported by the high level language.

However, the prior art sections of the instant application disclose (p. 2-7 of the specification) that vector operations, VLIW instruction, fused operations, specialization instructions were well known in the art at the time the invention was made. Therefore, it would have been obvious to one having ordinary skill in the art to incorporate the well known knowledge into the system of Jain et al to have the extension instructions containing various

types of instruction, such as vectorized versions of the existing instructions, or VLIW combinations of the existing instructions, or fused combinations of the existing instructions, or specialized versions of the existing instructions, or vectorized versions of operations supported by the high level language or VLIW combinations of operations supported by the high level language, or fused combinations of operations supported by the high level language or specialized versions of operations supported by the high level language, or at least two of vectorized, VLIW, fused and specialized versions of the existing instructions, or at least two of vectorized, VLIW, fused and specialized versions of operations supported by the high level language because one having ordinary skill in the art would want to utilize the technique as taught by Jain et al to optimize various types of instruction set architectures to meet the needs of various types of systems.

Claim 30 is rejected for the reasons set forth in the rejections of claim 1, 3 and 14.

Claim 31 is rejected for the reasons set forth in the rejections of claim 1, 2, 3 and 14.

Claim 32 is rejected for the reasons set forth in the rejections of claim 1, 6 and 14.

Claim 33 is rejected for the reasons set forth in the rejections of claim 1, 2, 3 and 14.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wei Y Zhen whose telephone number is (703) 305-0437. The examiner can normally be reached on Monday-Friday, 8 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on (703) 305-4552. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wei Zhen
Primary Examiner
9/1/2004